CLAIM AMENDMENT:

Please cancel claims 1-16 and add new claims 17-30.

Claims 1-16 (canceled)

Claim 17 (new): A method of manufacturing a semiconductor device, comprising:

preparing an SOI substrate;

forming a metal layer on the SOI substrate;

annealing the metal layer at a first temperature, which is effective in converting the metal layer into a first silicide layer;

forming an insulating layer on the first silicide layer; and

forming a hole from a surface of the insulating layer until a part of the first silicide layer is exposed; and

annealing the first silicide layer at a second temperature, which is effective in converting the first silicide layer into a second silicide layer wherein the second temperature is higher than the first temperature.

Claim 18 (new): A method as claimed in claim 17 wherein the metal layer includes cobalt.

Clam 19 (new): A method as claimed in claim 18 wherein the first silicide layer includes CoSi.

Clam 20 (new): A method as claimed in claim 19 wherein the second silicide layer includes $CoSi_2$.

Claim 21 (new): A method as claimed in claim 17 wherein annealing the metal layer is carried out by a rapid thermal annealing.

Claim 22 (new): A method as claimed in claim 21 wherein the rapid thermal annealing is carried out at a temperature in a range between about 450 ℃ and about 550 ℃.

Claim 23 (new): A method as claimed in claim 22 wherein the rapid thermal annealing is carried out at a temperature of about 550 ℃ for about 30 seconds.

Claim 24 (new): A method as claimed in claim 17 wherein annealing the first silicide layer is carried out by a rapid thermal annealing.

Claim 25 (new): A method as claimed in claim 24 wherein the rapid thermal annealing is carried out at a temperature of about 800 ℃.

Claim 26 (new): A method as claimed in claim 17 wherein the SOI substrate has a thickness of 50nm or less.

Claim 27 (new): A method as claimed in claim 17 wherein the hole has a diameter of 0.1 μm or less.

Claim 28 (new): A method as claimed in claim 17 wherein a time period of annealing the metal layer is shorter than that of annealing the first silicide layer.

Claim 29 (new): A method as claimed in claim 17 wherein a difference between the first temperature and the second temperature is 350 ℃ or less.

Claim 30 (new): A method as claimed in claim 17 wherein a resistance value of the first silicide layer is higher than that of the second silicide layer.